

FORM PTO-1449  U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE  LIST OF REFERENCES CITED BY APPLICANT  (Use several sheets if necessary)	ATTY. DOCKET NO. 58268.00368	SERIAL NO. New Cont. Appln
	APPLICANT Ning LI et al.	
	FILING DATE March 19, 2004	GROUP 2817

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
<i>gen</i>	AA	5,381,112	01-10-1995	Rybicki et al.	330	253	
<i>gen</i>	AB	6,107,882	08-22-2000	Gabara et al.	330	253	
<i>gen</i>	AC	6,326,815 B1	12-04-2001	Sim et al.	327	57	
<i>gen</i>	AD	20020008550 A1	01-24-2002	Sim et al.	327	57	09-18-2001
<i>gen</i>	AE	6,275,107 B1	08/14/01	Maeda et al.	330	253	
<i>gen</i>	AG	5,767,698	06/16/98	Emeigh et al.	326	53	
<i>gen</i>	AH	6,252,435 B1	06/26/01	Wu et al.	327	65	
<i>gen</i>	AI	6,118,438	09/12/00	Ho	345	204	
<i>gen</i>	AJ	6,525,607	02-25-03	Liu	330	253	

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION YES NO PART.		
<i>gen</i>	AK	DE 10022770 A1	02-08-2001	Germany				X	
	AL								

## OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

<i>gen</i>	AM	"LVDS I/O Interface of Gb/s-per-Pin Operation in 0.35- $\mu$ m CMOS" by Andrea Boni, Member, IEEE, Andrea Pierazzi, and Davide Vecchi; IEEE Journal of Solid-State Circuits, Vol. 36, No. 4, April 2001; pgs. 706-711
<i>gen</i>	AN	"Enhanced LVDS for Signaling on the RapidIO™ Interconnect Architecture", by Brian Young; Somerset Design Center, Motorola; pgs 17-20, March, 2000, IEEE, 0-7803-6450-3100
<i>gen</i>	AO	IEEE Standard for Low-Voltage; Annex A, Annex B and Annex C, 1996

EXAMINER <i>S J Mottola</i>	DATE CONSIDERED <i>7-7-04</i>
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.